A Single Amplifier-Based 12-bit 100 MS/s 1 V 19 mW 0.13 μm CMOS ADC with Various Power and Area Minimized Circuit Techniques

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SUMMARY This work describes a 12-bit 100 MS/s 0.13 μm CMOS three-stage pipeline ADC with various circuit design techniques to reduce power and die area. Digitally controlled timing delay and gate-bootstrapping circuits improve the linearity and sampling time mismatch of the SHA-free input network composed of an MDAC and a FLASH ADC. A single two-stage switched op-amp is shared between adjacent MDACs without MOS series switches and memory effects by employing two separate NMOS input pairs based on slightly overlapped switching clocks. The interpolation, open-loop offset sampling, and two-step reference selection schemes for a back-end 6-bit flash ADC reduce both power consumption and chip area drastically compared to the conventional 6-bit flash ADCs. The prototype ADC in a 0.13 μm CMOS process demonstrates measured differential and integral non-linearities within 0.44LSB and 1.54LSB, respectively. The ADC shows a maximum SNDR and SFDR of 60.5 dB and 71.2 dB at 100 MS/s, respectively. The ADC with an active die area of 0.92 mm² consumes 19 mW at 100 MS/s from a 1.0 V supply. The measured FOM is 0.22 pJ/conversion-step.

key words: ADC, pipeline, low power, SHA-free, circuit sharing, two-step reference selection

1. Introduction

Recently, the demand for high-performance A/D Converters (ADCs) has greatly increased for 3G communications, various display analog front-ends, and ultrasound imaging systems. The ADCs for such applications require more or less 12-bit resolution and a conversion rate exceeding 100 MS/s [1]–[5]. For diverse system-on-a-chip (SoC) applications, the ADCs also need to be power and area efficient. The pipeline architecture has been commonly employed to achieve the target specification with a good trade-off among speed, power consumption, and die area.

On the other hand, an op-amp is one of the most critical functional circuit blocks in the pipeline ADCs. The reduced dynamic voltage headroom and low output resistance of transistors make the op-amp design more strict, particularly, in low-voltage CMOS technologies. A two-stage op-amp has been widely adopted to obtain the required high voltage swing and DC gain [2], [5], [6], although considerable power is usually dissipated to push up the non-dominant pole to a high frequency region. Each pipeline stage requires an op-amp to amplify a residue voltage. Thus, the number of pipeline stages needs to be optimized in high-conversion rate and low-voltage pipeline ADCs.

Within the target conversion speed, a single-bit-per-stage architecture is relatively faster than a multi-bit-per-stage topology due to the high feedback factor. However, the single-bit-per-stage architecture needs more pipeline stages and non-dominant poles to be pushed up for a stable phase margin, resulting in less power efficiency. The multi-bit-per-stage architecture diminishes the above mentioned problems and optimizes power dissipation and chip area effectively with less pipeline stages [6], [7]. The number of pipeline stages can be decreased further by assigning more digital bits in the back-end sub-ranging flash ADCs. However, more bits in the flash ADC mean the exponentially increased number of comparators with a multi-stage pre-amp for a high DC gain considering the inevitable latch offsets [8]. Recently reported 12-bit pipeline ADCs have employed more than four stages with 3 or 4 bits per stage [2], [6], [9].

In this work, the proposed 12-bit ADC is based on three pipeline stages deciding 4, 4, and 6 bits, respectively, with only one op-amp to minimize power consumption [10] and chip area drastically with this specific CMOS process. A conventional dedicated input sample-and-hold amplifier (SHA) is not employed in the proposed ADC. A sampling time mismatch between the first-stage multiplying D/A converter (MDAC) and the first-stage flash ADC is removed with digitally controlled time delay and gate-bootstrapping circuits [11], [12]. Only one high-speed op-amp is employed in the whole ADC and shared between two adjacent MDACs. Two separated NMOS differential input pairs of the shared op-amp remove a memory effect while two slightly overlapped switching clocks achieve a fast signal settling. Moreover, two-step reference selection and interpolation schemes for the last stage 6-bit flash ADC reduce the number of pre-amps to 50% compared to the conventional interpolated 6-bit flash ADCs.

The architecture of the proposed ADC is described in Sect. 2, while detailed circuit design techniques are discussed in Sect. 3. The measured performance of the prototype ADC is summarized in Sect. 4 and Sect. 5 concludes this paper.

2. Proposed ADC Architecture

The proposed 12-bit ADC with three pipeline stages needs
only one shared op-amp as illustrated in Fig. 1. The conventional front-end high-speed input SHA is not employed here, while the first and second stages decide 4 bits followed by the remaining 6 bits from the back-end flash ADC, FLASH3. A switched op-amp is shared for two 4-bit MDACs, MDAC1 and MDAC2, optimizing the required specifications during each MDAC operation such as DC gain, $f_{3dB}$, power dissipation, and phase margin. Two NMOS differential input pairs properly handle each MDAC signal with alternative switched operation while removing a memory effect. A bit overlapped switching clock phase for signal selection switches minimizes an output signal settling delay, as observed in the conventional switched op-amp sharing technique [13]. A capacitor scaling [14] for each pipeline stage and a cascode compensation technique [2] for the shared two-stage op-amp save more power consumption and chip area.

A resistor ladder is also shared for the front-end two 4-bit flash ADCs and an interpolation technique is used in all the flash ADCs. In the last-stage 6-bit flash ADC, a two-step reference selection scheme removes the conventional flash ADC problem, which is the exponential increasement of power consumption and chip area with an increasing resolution. Current and voltage reference generator, digital correction logic with a decimator circuit, and clock generator are implemented on chip for various SoC applications. The clock generator produces two non-overlapped clocks, Q1 and Q2, from an external reference clock. Two slightly overlapped clock phases, Q1B and Q2B, steer the corresponding current for each MDAC operation of the shared switched op-amp.

3. Circuit Implementation

3.1 SHA-Free Input Network with High Sampling Accuracy

High-resolution high-speed ADCs commonly employ an input SHA to deliver a sampled input to the first-stage MDAC and flash ADC. The input SHA tends to consume considerable power in the op-amp to achieve the required performance such as DC gain, bandwidth, accuracy, noise, and operating speed. The proposed ADC employs an SHA-free architecture and analog inputs are sampled on the capacitors of the first-stage MDAC and flash ADC directly. In the conventional SHA-free ADCs, a sampled signal mismatch can occur due to a different signal delay time between the first-stage MDAC and the first flash ADC using pre-amps and this tends to limit the signal bandwidth [11]. This sampled signal mismatch can be reduced with the same gate-bootstrapping circuit for the sampling switches of the first-stage MDAC and flash ADC, as shown in Fig. 2.

The gate-bootstrapping circuit minimizes the input dependent $V_{GS}$ variation of sampling switches by maintaining the on resistance, $R_{ON}$, constant. Thus, the sampled signal mismatch is a lot reduced by adjusting the size ratio of capacitors and switches in the input network. A designed and simulated gate-bootstrapping circuit achieves an accuracy exceeding 12 bits with low distortion using a 1.0 V supply.

On the other hand, the 4-bit FLASH1 ADC needs a pre-amp to reduce the kick-back effect and the input referred static and dynamic offsets of the latch circuit, while the pre-amp needs a time to amplify a voltage difference between an input and a specified reference voltage during the amplifying time interval. The proposed SHA-free input network employs Q1X to sample an input and Q1Y to amplify the difference of the sampled input and a reference from the resistor ladder of the FLASH1 ADC. Two clock phases, Q1X and Q1Y, are approximately corresponding to a half period of Q1, as shown in Fig. 3. The next amplifying period, Q2, of the MDAC1 is identical to the conventional SHA-based architecture and there is no additional power dissipation.

The extra timing phases have been generated with an external system clock exceeding the target conversion rate in [15]. In the proposed SHA-free input network, digitally controlled timing delay circuits based only on a single 100 MHz system clock generate Q1X and Q1Y, as shown Fig. 4. When the 3-bit digital control signal is “100”, the delay time ($t_d$) of Q1X is approximately set to a half of Q1. Considering process, voltage, and temperature variations, the manually controlled 3-bit digital signal can vary from “000” to “111” and control the delay time within ±20% from a half of Q1.
3.2 MDAC Sharing Scheme Based on a Switched op-amp to Remove Series Switches and Memory Effects

Considering an op-amp usually amplifies only during a half clock cycle in pipeline ADCs, the shared and switched op-amp techniques have been widely used for various op-amp applications [16]–[19]. In this work, a two-stage op-amp with cascode compensation is implemented to obtain a high DC gain of 84 dB for a 12-bit resolution, a phase margin of 63° for stability, a wide bandwidth for 100 MS/s and a 1 Vp-p signal swing range at a 1.0 V power supply, as shown in Fig. 5. Although a single-ended circuit topology is illustrated for simplicity, the actual circuit is implemented in a fully differential version.

In the whole ADC, the proposed two-stage switched op-amp is employed only once and shared for the merged MDAC of MDAC1 and MDAC2 to save power consumption. A memory effect due to the remaining charge from the previous phase, as observed in the conventional op-amp sharing circuits, does not occur in the proposed op-amp. The input pair not being used for amplification is always reset to the signal common.

During Q1, the input pair for the MDAC1 is reset to the signal common and the MDAC1 capacitors, C_{S1} \langle 1:8 \rangle, sample an analog input, V_{in}, while the MDAC2 amplifies a residue voltage. During the next Q2, the input pair for the MDAC2 is reset to the common and the MDAC1 amplifies a residue voltage, while the MDAC2 capacitors, C_{S2} \langle 1:7 \rangle and C_{F2}, sample the amplified residue voltage of the MDAC1. The sampling capacitances in the MDAC1 and MDAC2 are 1.6 pF and 0.8 pF, respectively.

The detailed circuit diagram of the proposed two-stage op-amp is illustrated in Fig. 6. The shared op-amp consists of two separate NMOS differential input pairs in the first-stage amplifier. The input transistor pairs are turned on and off alternately by using the switches with slightly overlapped clocks, Q1B and Q2B. The first and second stages of the two-stage amplifier employ independent switched-capacitor type common-mode feedback circuits for low power, which are now shown in Fig. 6 for simplicity.

The switches for two NMOS input pairs are controlled by two overlapped clocks, Q1B and Q2B. Figures 7(a) and 7(b) describe both the non-overlapped and overlapped clock phases. During the slightly overlapped time interval of Q1B and Q2B, both of the NMOS input pairs are simultaneously turned on just before the amplifying phase to get the fast output signal settling. When Q2 and Q1 rather than Q1B and Q2B are employed to select each NMOS input pair, both of
the current paths are cut off during the short non-overlapped time period and all of the NMOS input pairs are also turned off. As a result, during the next amplifying phase, it takes a time to turn on the NMOS input pair being used, which delays the output signal settling. The overlapped time interval can be controlled with the number and size of digital buffers.

3.3 Back-End 6-Bit Flash ADC Based on a Two-Step Reference Selection Scheme

A flash ADC is one of key circuit components for various forms of the ADCs to convert analog signals to digital outputs based on a fast conversion rate and a simple architectural characteristic. The flash ADC is also employed for residue amplification in each stage of the pipeline ADC, but the number of comparators is increased exponentially with a specified resolution, which is a major disadvantage of the flash ADC. In this work, the proposed 6-bit flash ADC in the last pipeline stage employs an interpolation technique and a two-step reference selection scheme. The interpolation reduces the number of pre-amps in the flash ADC by 50%. The two-step reference selection scheme further reduces the number of all the comparators required in the 6-bit flash ADC by 50%. The proposed reference selection first decides the most significant bit (MSB), then the 5-bit least significant bits (LSBs) depending on the MSB result, as shown in Fig. 8.

In the first clock phase, a mid-point comparator, COMPM, samples a mid-point reference voltage, REFMID. In the next clock phase, the COMPM compares the sampled REFMID with an analog input (\(V_{IN}\)) and generates the digital MSB, OUTM, while the comparators, COMPLs, for the 5-bit LSBs, sample the same \(V_{IN}\). In the subsequent clock phase, separate reference voltages for the COMPLs are selected by the OUTM while the COMPLs compare each selected reference voltage with \(V_{IN}\) to generate the remaining 5-bit LSBs.

As for the timing sequence, the conventional flash ADC based on the two-step sub-ranging reference scheme needs an additional clock period faster than the conversion rate, which results in more power consumption [20]. Since the flash ADC with the proposed two-step reference selection is integrated in the last pipeline stage, extra timing is not needed. Only a change of sampling order of input and reference and a half clock pipeline delay are sufficient. The detailed pipeline timing sequence is summarized in Fig. 9.

The detailed circuit of COMPL in Fig. 8 is shown in Fig. 10. The signals, Q2T, Q2TB, Q2C, and Q2CB, for reference selection, are generated by simple digital logic gates with the OUTM and two clock signals, Q2 and Q2B. A two-stage pre-amp with open-loop offset cancellation is used to obtain the required 6-bit resolution. The proposed two-step reference selection technique combined with the interpolation scheme drastically decrease power consumption and chip area with the reduced number of comparators, when compared to the conventional 6-bit flash ADCs.

4. Prototype ADC Measurements

The proposed 12-bit 100 MS/s pipeline ADC is implemented in two versions based on a 0.13 \(\mu\)m CMOS process, occupying an active area of 0.92 mm\(^2\) as shown in Fig. 11. The Version 1 (V1) ADC employing an SHA and the Version 2 (V2) ADC without any SHA are simultaneously implemented and their performances are measured and compared. In the V2 ADC, the space surrounded by a dashed line corresponding to the SHA circuit of the V1 ADC. The removed SHA block for the V2 ADC is occupied by by-pass capacitors of 160 pF for power supplies. The on-chip NMOS and PMOS capacitors of 420 pF in the idle space of the V2 ADC reduce the signal interference between functional blocks, EMI, power supply noise, and high-speed transient glitches.
The prototype ADC dissipates 24 mW and 19 mW for V1 and V2, respectively, with a conversion rate of 100 MS/s at a 1.0 V supply. The 3-bit digital timing control signal is manually set “111”, which is the longest sampling time and shows the best performance. The measured differential non-linearity (DNL) and integral non-linearity (INL) are within 0.44LSB and 1.54LSB, respectively, as illustrated in Fig. 12.

An FFT signal spectrum at 100 MS/s with a 4 MHz input sine wave and a 1.0 V supply voltage is plotted in Fig. 13. Digital output data are captured at a quarter rate of the full conversion speed of 100 MS/s by the on-chip decimator.

The signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) in Fig. 14(a) are measured with increasing sampling frequencies at an input frequency of 4 MHz. When the sampling frequency is increased up to 100 MS/s, the SNDR and SFDR are maintained above 60 dB and 71 dB at 1.0 V, respectively. The SNDR of the V2 ADC is slightly higher than the V1 ADC. It means that the absence of the input SHA lowers the noise floor a little bit. On the contrary, the SFDR of the V1 ADC is higher than that of the V2 ADC with an input SHA. On the other hand, Fig. 14(b) shows the SNDR and SFDR variations with increasing input frequencies at a maximum sampling frequency of 100 MS/s. As input frequencies are increasing, the difference of dynamic performances between two versions of ADCs grows bigger. A front-end SHA circuit is required for applications processing high-frequency input signals.

The performance of the prototype ADC is summarized in Table 1. The proposed ADC is compared with recently reported 12-bit 100 MS/s-level CMOS ADCs in Table 2. The well-known figure-of-merits (FOMs) defined as (1) and (2) are 0.22 pJ/conversion-step and 1.22 pJ/conversion-step, respectively.

\[
FOM^1 = \frac{\text{power}}{f_s \times 2^{\text{ENOB}}} \quad (1)
\]

\[
FOM^2 = \frac{\text{power}}{(2 \times \text{ERBW}) \times 2^{\text{ENOB}}} \quad (2)
\]

5. Conclusion

This work proposes a 12-bit 100 MS/s 0.13 µm CMOS
pipeline ADC with various power and area minimized circuit techniques based on a single op-amp. Digitally controlled timing delay and gate-bootstrapping circuits improve the sampling time mismatch of the SHA-free first pipeline stage composed of an MDAC and a FLASH ADC. A single shared and switched op-amp with two separated NMOS input pairs for two MDACs removes MOS series switches and memory effects for a fast signal settling. The interpolation and two-step reference selection schemes for the last-stage 6-bit flash ADC reduce both power consumption and chip area drastically compared to the conventional 6-bit flash ADCs. The prototype ADC in 0.13 µm CMOS shows the measured DNL and INL within 0.44 LSB and 0.58 LSB, respectively. The ADC with an active die area of 0.92 mm² consumes 19 mW at 1.0 V supply and 100 MS/s.

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References


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Table 1  Performance summary of the prototype ADC.

| Resolution | 12bits |
| Conversion rate | 100MS/s |
| Process | 0.13µm CMOS |
| Supply voltage | 1.0V |
| Input range | 1.0Vp-p |
| Reference Voltage | V1 (w/ SHA) | V2 (w/o SHA) |
| S/N (at f_0 = 4MHz) | 60.23dB | 60.53dB |
| SFDR (at f_0 = 4MHz) | 73.43dB | 71.22dB |
| DNLS | -0.40LSB/0.34LSB | -0.38LSB/0.44LSB |
| INLs | -0.91LSB/1.79LSB | -1.54LSB/1.43LSB |
| Power consumption | SHA | 5.0mW |
| MDAC | 11.6mW |
| FLASH | 3.7mW |
| I/V REF | 2.0mW |
| DCL/CLOCK/CM | 1.7mW |
| TOTAL | 24mW | 19mW |
| Area | 0.92mm² (= 0.91mm × 1.01mm) |

Table 2  Performance comparison of recently reported 12-bit CMOS ADCs operating at 100 MS/s level.

<table>
<thead>
<tr>
<th>Speed (MS/s)</th>
<th>Power (mW)</th>
<th>Area (mm²)</th>
<th>Supply (V)</th>
<th>DNL/INL (LSB)</th>
<th>FOM* (pJ/Chip)</th>
<th>FOM* (pJ/Chip)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC V1 100</td>
<td>24</td>
<td>0.92</td>
<td>0.40/0.19</td>
<td>0.29</td>
<td>0.29</td>
<td></td>
</tr>
<tr>
<td>ADC V2 100</td>
<td>19</td>
<td>0.32</td>
<td>0.60/0.20</td>
<td>0.05</td>
<td>0.50</td>
<td></td>
</tr>
<tr>
<td>ADC 100</td>
<td>42</td>
<td>1.22</td>
<td>0.38/0.96</td>
<td>0.31</td>
<td>0.65</td>
<td></td>
</tr>
<tr>
<td>ADC 100</td>
<td>55</td>
<td>5.78</td>
<td>1.0/0.34</td>
<td>0.67</td>
<td>1.04</td>
<td></td>
</tr>
<tr>
<td>ADC 110</td>
<td>97</td>
<td>0.86</td>
<td>1.20/1.30</td>
<td>0.67</td>
<td>1.49</td>
<td></td>
</tr>
<tr>
<td>ADC 120</td>
<td>52</td>
<td>0.56</td>
<td>1.30/0.95</td>
<td>0.46</td>
<td>0.46</td>
<td></td>
</tr>
<tr>
<td>ADC 120</td>
<td>42</td>
<td>0.38</td>
<td>0.60/0.20</td>
<td>0.05</td>
<td>0.50</td>
<td></td>
</tr>
<tr>
<td>ADC 120</td>
<td>32</td>
<td>1.20</td>
<td>0.38/0.96</td>
<td>0.31</td>
<td>0.65</td>
<td></td>
</tr>
<tr>
<td>ADC 120</td>
<td>55</td>
<td>1.00</td>
<td>0.34/0.70</td>
<td>0.70</td>
<td>1.04</td>
<td></td>
</tr>
<tr>
<td>ADC 120</td>
<td>80</td>
<td>1.20</td>
<td>1.30/1.50</td>
<td>0.67</td>
<td>1.49</td>
<td></td>
</tr>
<tr>
<td>ADC 120</td>
<td>100</td>
<td>1.50</td>
<td>0.95/1.05</td>
<td>0.46</td>
<td>0.46</td>
<td></td>
</tr>
<tr>
<td>ADC 120</td>
<td>120</td>
<td>2.00</td>
<td>1.30/1.50</td>
<td>0.67</td>
<td>1.49</td>
<td></td>
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</tbody>
</table>


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